Auto-vectorization in Graal
Graal Workshop @ CGO 2020

Our journey implementing Auto-vectorization in Graal CE on the #TwitterVMTeam

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Talk Outline

1. Autovectorization recap
2. Implementation
3. Challenges
4. Examples and Benchmarks
5. Conclusion
Autovectorization Recap
Auto-vectorization Recap

- Modern processors feature registers that hold vectors of values and have vector arithmetic operations.
- Analyze a program and find the vectors.
- Generate vector instructions.
- Usually found in loops.
void addMyArrays(int[] a, int[] b, int[] c) {
    for (int i = 0; i < 100; i++) {
        c[i] = a[i] + b[i];
    }
}
void addMyArrays(int[] a, int[] b, int[] c) {
    for (int i = 0; i < 100; i+=4) {
        c[i:i+4] = a[i:i+4] + b[i:i+4];
    }
}
Autovectorization Recap: An Example

Scalar

```
... 
add [rax], 1
add [rax + 4], 2
add [rax + 8], 3
add [rax + 12], 4
... 
```

Vector

```
... 
movdqu xmm1, 0xf12937b0
movdqu xmm0, [rax]
paddd xmm0, xmm1
movdqu [rax], xmm0
... 
```
Implementation
Exploiting Superword Level Parallelism with Multimedia Instruction Sets

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Abstract
Increasing focus on multimedia applications has prompted the addition of multimedia extensions to most existing general-purpose microprocessors. The added functionality comes primarily with the addition of short SIMD instructions. Unfortunately, access to these instructions is limited to in-line assembly and library calls. Generally, it has been assumed that vector codes provide the most promising means of exploiting multimedia instructions. Although vectorization technology is well understood, it is inherently complex and fragile. In addition, it is incapable of locating SIMD-style parallelism within a basic block.

In this paper we introduce the concept of Superword Level Parallelism (SLP), a novel way of viewing parallelism in multimedia and scientific applications. We believe SLP is fundamentally different from the loop level parallelism exploited by traditional vector processing, and therefore demands a new method of exploiting it. We have developed a simple and robust compiler for detecting SLP that targets basic blocks rather than loop nests. As such, it is a technique to exploit both across loop iterations and within basic blocks. The result is an algorithm that provides excellent performance in several application domains. In our experiments, dynamic instruction counts were reduced by 40%. Speedups ranged from 1.24 to 6.70.

1 Introduction

The recent shift toward computation-intensive multimedia workloads has resulted in a variety of new multimedia extensions to current microprocessors [6, 10, 15, 18, 20]. Many new designs are targeted specifically at the multimedia domain [8, 7, 11]. This trend is likely to continue as it has been projected that multimedia processing will soon become the main focus of microprocessor design.8

While different processors vary in the type and number of multimedia instructions offered, the core of each is a short SIMD or superword operation. These instructions operate concurrently on data that are packed in a single register or memory location. In the past, such systems could accommodate only small data types of 8 or 16 bits, making them suitable for a limited set of applications. With the emergence of 128-bit superwords, new architectures are capable of performing four 32-bit operations with a single instruction. By adding floating point support as well, these extensions can now be used to perform more general purpose computation.

It is not surprising that SIMD execution units have appeared in desktop microprocessors. Their simple control, replicated functional units, and absence of lengthy register file entries make them inherently simple and extremely amenable to scaling. As the number of available transistors increases with advances in semiconductor technology, datapaths are likely to grow even larger.

Today, use of multimedia extensions is difficult since application writers are largely restricted to using in-line assembly routines or specialized library calls. The problem is exacerbated by inconsistencies among different instruction sets. One solution to this incompatibility is to employ vectorization techniques that have been used to parallelize scientific code for vector machines [9, 14, 15]. Since a number of multimedia applications are vectorizable, this approach promises good results. However, many important multimedia applications are difficult to vectorize. Complicated loop transformation techniques such as loop fusion and inner expansion are required to parallelize loops that are only partially vectorizable [2, 4, 17]. Consequently, no commercial compiler currently implements this functionality. This paper presents a method for extracting SIMD parallelism beyond vectorizable loops.

We believe that short SIMD operations are well suited to exploit a fundamentally different type of parallelism than the vector parallelism associated with traditional vector and SIMD supercomputers. We denote this parallelism Superword Level Parallelism (SLP) since it comes in the form of superwords containing packed data. Vector supercomputers require large amounts of parallelism in order to achieve speedups, whereas SLP can be profitable when parallelism is scarce. From this perspective, we have developed a general algorithm for detecting SLP that targets basic blocks rather than loop nests.

In some respects, superword level parallelism is a restricted form of SLP. ILP techniques have been very successful in the general purpose computing arena, partly because of their ability to find parallelism within basic blocks. In the same way that loop unrolling translates loop level parallelism into ILP, vector parallelism can be transformed into SLP. This realization allows for the parallelization of vector-

Available from:
The Algorithm

For each basic block:

1. Pair isomorphic instructions containing adjacent memory references.
2. Extend set of pairs by finding instructions using def-use chains and def-use chains of step 1 pairs.
3. Combine the pairs into a set of adjacent packs, until the set no longer changes.
4. Schedule packs for execution.

\[
\begin{align*}
    c &= a + b & \quad & \text{Isomorphic} \\
    d &= e + f & \quad & \text{Independent} \\

    c &= a + b & \quad & \text{Isomorphic} \\
    d &= c + f & \quad & \text{Independent}
\end{align*}
\]
The Algorithm

For each basic block:

1. **Pair isomorphic instructions containing adjacent memory references.**
2. Extend set of pairs by finding instructions using def-use chains and def-use chains of step 1 pairs.
3. Combine the pairs into a set of adjacent packs, until the set no longer changes.
4. Schedule packs for execution.

**Program**

1. $b = a[i+0]$
2. $c = 5$
3. $d = b + c$
4. $e = a[i+1]$
5. $f = 6$
6. $g = e + f$
7. $h = a[i+2]$
8. $j = 7$
9. $k = h + j$

**Packed Set**

{ (1, 4), 
  (4, 7), 
}
The Algorithm

For each basic block:

1. Pair isomorphic instructions containing adjacent memory references.
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Program

(1) b = a[i+0]
(2) c = 5
(3) d = b + c
(4) e = a[i+1]
(5) f = 6
(6) g = e + f
(7) h = a[i+2]
(8) j = 7
(9) k = h + j

Packed Set

{ (1, 4),
  (4, 7),
  (3, 6), // u-d
  (6, 9), // u-d
  (2, 5), // d-u
  (5, 8), // d-u
}

E.g. (1, 4) defines b and e, which are used by (3, 6).
(3, 6) uses c and f, which are defined by (2, 5).
The Algorithm

For each basic block:

1. Pair isomorphic instructions containing adjacent memory references.
2. Extend set of pairs by finding instructions using def-use chains and def-use chains of step 1 pairs.
3. **Combine the pairs into a set of adjacent packs, until the set no longer changes.**
4. Schedule packs for execution.

Program

```
(1) b = a[i+0]
(2) c = 5
(3) d = b + c
(4) e = a[i+1]
(5) f = 6
(6) g = e + f
(7) h = a[i+2]
(8) j = 7
(9) k = h + j
```

Packed Set

```
{ (1, 4, 7),
  (3, 6, 9),
  (2, 5, 8)
}
```
The Algorithm

For each basic block:

1. Pair isomorphic instructions containing adjacent memory references.
2. Extend set of pairs by finding instructions using def-use chains and def-use chains of step 1 pairs.
3. Combine the pairs into a set of adjacent packs, until the set no longer changes.
4. **Schedule packs for execution.**

<table>
<thead>
<tr>
<th>Program</th>
<th>Vectorized Program</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) ( b = a[i+0] )</td>
<td>( d \quad a[i+0] \quad 5 )</td>
</tr>
<tr>
<td>(2) ( c = 5 )</td>
<td>( g = a[i+1] + 6 )</td>
</tr>
<tr>
<td>(3) ( d = b + c )</td>
<td>( k \quad a[i+2] \quad 7 )</td>
</tr>
<tr>
<td>(4) ( e = a[i+1] )</td>
<td></td>
</tr>
<tr>
<td>(5) ( f = 6 )</td>
<td></td>
</tr>
<tr>
<td>(6) ( g = e + f )</td>
<td></td>
</tr>
<tr>
<td>(7) ( h = a[i+2] )</td>
<td></td>
</tr>
<tr>
<td>(8) ( j = 7 )</td>
<td></td>
</tr>
<tr>
<td>(9) ( k = h + j )</td>
<td></td>
</tr>
</tbody>
</table>
Algorithm Alternatives

Why SLP?

- A starting point.
- Tried and tested, implemented in C2 and LLVM to different extents.
- Later literature builds on top of SLP.
  - Bottom-up SLP
  - VW-SLP
  - etc
The Algorithm: Implementation

IsomorphicPackingPhase

Vector Stamps

VectorReadNode / VectorWriteNode

VectorExtractNode / VectorPackNode

Scheduling + Canonicalization
Phase Ordering

IsomorphicPackingPhase invoked in LowTier

Low tier features general memory ops.

Low tier means fewer passes need to support vector stamps.
Interface to Code Generator

Three new methods in LIRGeneratorTool

- emitPackConst
- emitPack
- emitExtract

Otherwise, we reuse existing emits

- emitAdd
- emitXor
- etc...
## Supported Operations

<table>
<thead>
<tr>
<th>Arithmetic</th>
<th>Packing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integer</td>
<td>Float</td>
</tr>
<tr>
<td>Add</td>
<td>Add</td>
</tr>
<tr>
<td>Subtract</td>
<td>Subtract</td>
</tr>
<tr>
<td>Multiply</td>
<td>Multiply</td>
</tr>
<tr>
<td>And</td>
<td>Divide</td>
</tr>
<tr>
<td>Or</td>
<td>Remainder</td>
</tr>
<tr>
<td>Xor</td>
<td>Negate</td>
</tr>
<tr>
<td>Negate</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Load</td>
</tr>
<tr>
<td></td>
<td>Store</td>
</tr>
<tr>
<td></td>
<td>Constant Pack</td>
</tr>
<tr>
<td></td>
<td>Insert</td>
</tr>
<tr>
<td></td>
<td>Extract</td>
</tr>
</tbody>
</table>
Stack Packing

```c
uint32_t foo1(__m256i vec, int j)
{
    return (uint32_t)__mm256_extract_epi32(vec, j);
}
```

Clang 5.0 intrinsic.
(viewed using [godbolt.org](https://godbolt.org))

Aligns stack pointer and allocates space.

Extracts a single element from the vector.

```
and rsp, -32
sub rsp, 64
and edi, 7
vmovaps ymmword ptr [rsp], ymm0
mov eax, dword ptr [rsp + 4*rdi]
mov rsp, rbp
```
Challenges
Heuristics

- Too much vectorization is bad.
- Heuristics let us know if a part of the code should be vectorized.
Loop Unrolling & Bounds Check Elimination

- Graal features bounds checks for array accesses.
- Disables loop unrolling!
- Hacks around this:
  - Unroll earlier, before guards are lowered.
  - Remove bounds checks.
Bug: String Hashcode

The Problem: Memory corruption in strings, lots of NoSuchMethodErrors.

Location: Traced to a hashCode() method for Latin1 strings.

Cause: Emitting instructions using the stack kind instead of platform-specific kind.

Solution: Use platform-specific kind instead.
Bug: Stack Pointer Addressing

**The Problem:** More memory corruption in strings!

**Location:** Traced to part of the regex matcher implementation.

**Cause:** Using the previously-mentioned stack loads and stores, rsp-relative addressing gets broken.

**Solution:** Replace dynamic use of stack pointer with a stack slot.
Bug: Floating-Point Extraction

The Problem: Data corruption, invalid results from vectorized floating point operations.

Location: AMD64 Assembler.

Cause: VPEXTRQ does not support XMM destination registers.

Solution: Check the register type and emit VPSHUFD if the destination register is of XMM type.
Examples and Benchmarks
Sample Code

```
for (int i = 0; i < count; i++) {
    tmp[i] = buf[i];
}
```

Excerpt from regex.Pattern#atom.

```
vmovdqu ymm0, YMMWORD PTR [r11+r10*4+0x10]
vmovdqu YMMWORD PTR [r14+r10*4+0x10], ymm0
```
Excerpt from SHA#implCompress0.

```
for (int t = 16; t <= 79; t++) {
    W[t] = (temp << 1) | (temp >>> 31);
}
```
Ionut Benchmarks

Sample Benchmarks (OpenJDK 14-ea+21-927 64-bit Server VM)

Credit to Ionuț Baloșin’s JVM JIT Performance Benchmarks.
Scimark

Scimark Benchmarks (OpenJDK 14-ea+21-927 64-bit Server VM)

- C2 (No Superword)
- C2 (Superword)
- Graal (No AV)
- Graal (No AV, No Bounds Check)
- Graal (AV, No Bounds Check)
Conclusion
Overall

- Autovectorization is hard.
- **Heuristics** make or break an implementation.
- Not all **requirements** are necessarily implemented already or foreseeable.
  - Bounds check elimination is really important.
Overall

The pull request: https://github.com/oracle/graal/pull/1692

Contribute: https://github.com/usrinivasan/graal

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